

PLUS Search Results for S/N 09787353, Searched January 25, 2005

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09787353_CLS
Most Frequently Occurring Classifications of Patents Returned
From A Search of 09787353 on January 25, 2005

Original Classifications

3 710/110
3 710/118
2 710/100
2 710/105
2 710/107
2 710/112
2 710/266
2 710/306

Cross-Reference Classifications

4 710/107
4 710/110
3 710/113
2 370/376
2 709/237
2 710/100
2 710/105
2 710/118
2 710/269
2 711/145
2 711/146
2 711/150
2 711/169

Combined Classifications

7 710/110
6 710/107
5 710/118
4 710/100
4 710/105
4 710/113
3 710/266
3 711/145
2 370/376
2 370/535
2 700/2
2 709/237
2 710/112
2 710/269
2 710/306
2 711/141
2 711/144
2 711/146
2 711/149
2 711/150
2 711/169
2 714/24
2 714/805

09787353_CLSTITLES
Titles of Most Frequently Occurring Classifications of Patents Returned
From A Search of 09787353 on January 25, 2005

- 7 710/110 (3 OR, 4 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/110 ..Bus master/slave controlling
- 6 710/107 (2 OR, 4 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
TRANSACTION PROCESSING)
710/107 .Bus access regulation
- 5 710/118 (3 OR, 2 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/113 ..Centralized bus arbitration
710/118 ...Delay reduction
- 4 710/100 (2 OR, 2 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
TRANSACTION PROCESSING)
- 4 710/105 (2 OR, 2 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
TRANSACTION PROCESSING)
710/105 .Protocol
- 4 710/113 (1 OR, 3 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/113 ..Centralized bus arbitration
- 3 710/266 (2 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
PROCESSING SYSTEMS: INPUT/OUTPUT
710/260 INTERRUPT PROCESSING
710/266 .Programmable interrupt processing
- 3 711/145 (1 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/141 ...Coherency
711/145Access control bit

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- 2 370/376 (0 OR, 2 XR)
 Class 370 : MULTIPLEX COMMUNICATIONS
 370/351 PATHFINDING OR ROUTING
 370/357 .Through a circuit switch
 370/360 ..Switching control
 370/375 ...Time switch, per se (e.g., T or T-T)
 370/376Time slot interchange, per se
- 2 370/535 (1 OR, 1 XR)
 Class 370 : MULTIPLEX COMMUNICATIONS
 370/473 ..Transmission of a single message having
 multiple packets
 370/498 .Combining or distributing information via time
 channels
 370/535 ..Multiplexing combined with demultiplexing
- 2 700/2 (1 OR, 1 XR)
 Class 700 : DATA PROCESSING: GENERIC CONTROL SYSTEMS OR
 SPECIFIC APPLICATIONS
 700/1 GENERIC CONTROL SYSTEM, APPARATUS OR PROCESS
 700/2 .Plural processors
- 2 709/237 (0 OR, 2 XR)
 Class 709 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
 SYSTEMS: MULTIPLE COMPUTER OR PROCESS COORDINATING
 709/200 MULTICOMPUTER DATA TRANSFERRING
 709/230 .Computer-to-computer protocol implementing
 709/237 ..Computer-to-computer handshaking
- 2 710/112 (2 OR, 0 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
 TRANSACTION PROCESSING)
 710/107 .Bus access regulation
 710/112 ..Bus request queuing
- 2 710/269 (0 OR, 2 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/260 INTERRUPT PROCESSING
 710/269 .Handling vector
- 2 710/306 (2 OR, 0 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
 TRANSACTION PROCESSING)
 710/305 .Bus interface architecture
 710/306 ..Bus bridge
- 2 711/141 (1 OR, 1 XR)
 Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
 SYSTEMS: MEMORY
 711/100 STORAGE ACCESSING AND CONTROL
 711/117 .Hierarchical memories
 711/118 ..Caching
 711/141 ...Coherency
- 2 711/144 (1 OR, 1 XR)
 Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
 SYSTEMS: MEMORY

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711/100	STORAGE ACCESSING AND CONTROL
711/117	.Hierarchical memories
711/118	..Caching
711/141	...Coherency
711/144Cache status data bit
2 711/146	(0 OR, 2 XR)
Class 711 :	ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
	SYSTEMS: MEMORY
711/100	STORAGE ACCESSING AND CONTROL
711/117	.Hierarchical memories
711/118	..Caching
711/141	...Coherency
711/146Snooping
2 711/149	(1 OR, 1 XR)
Class 711 :	ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
	SYSTEMS: MEMORY
711/100	STORAGE ACCESSING AND CONTROL
711/147	.Shared memory area
711/149	..Multiport memory
2 711/150	(0 OR, 2 XR)
Class 711 :	ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
	SYSTEMS: MEMORY
711/100	STORAGE ACCESSING AND CONTROL
711/147	.Shared memory area
711/150	..Simultaneous access regulation
2 711/169	(0 OR, 2 XR)
Class 711 :	ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
	SYSTEMS: MEMORY
711/100	STORAGE ACCESSING AND CONTROL
711/167	.Access timing
711/169	..Memory access pipelining
2 714/24	(1 OR, 1 XR)
Class 714 :	ERROR DETECTION/CORRECTION AND FAULT
	DETECTION/RECOVERY
714/100	DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING
714/1	.Reliability and availability
714/2	..Fault recovery
714/24	...Safe shutdown
2 714/805	(1 OR, 1 XR)
Class 714 :	ERROR DETECTION/CORRECTION AND FAULT
	DETECTION/RECOVERY
714/699	PULSE OR DATA ERROR HANDLING
714/799	.Error/fault detection technique
714/800	..Parity bit
714/805	...Storage accessing (e.g., address parity check)